Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 [CURRENTLY AMENDED] A circuit comprising a first terminal for connection to a voltage source having first and second levels and a transition between the levels, a driver including first and second opposite conductivity type transistors, said first and second transistors being respectively a PFET and an NFET, each of said transistors including a gate electrode and a source drain path arranged to be switched on and off in response to ~~the control electrode~~ a voltage applied to the gate electrode being on opposite sides of a threshold, the first and second transistor paths being connected in series across opposite power supply terminals, and pulse shaping circuitry for (a) causing the first and second ~~transistor~~ source drain paths to be respectively (i) on and off while the voltage source has the first level and (ii) off and on while the voltage source has the second level, and (b) preventing both source drain paths from being on simultaneously, the circuitry including a ~~first~~ resistive element and capacitor, the ~~first~~ resistive element being connected for supplying current to the capacitor and the gate electrode of the first transistor, the capacitor being connected across the gate electrode of one of said transistors and a first of the power supply terminals, the first power supply terminal being connected for supplying current to the source drain path of the other of said transistors while the source drain path of the other of said transistors is on, the capacitor comprising a field effect device having a conductivity type opposite to the conductivity type of said one of said transistors.

Claim 2 [CANCELED]

Claim 3 [CURRENTLY AMENDED] The circuit of claim 1 wherein said ~~first~~ resistive element, PFET, NFET and said capacitor are included on an integrated circuit chip, and said ~~first~~ resistive element comprises a resistor.

Claim 4 [CANCELED]

Claim 5 [CANCELED]

Claim 6 [CANCELED]

Claim 7 [CURRENTLY AMENDED] The circuit of claim ~~5~~ 1 wherein the pulse shaping circuitry includes a ~~first and second~~ switching ~~circuits each~~ circuit having (a) an input terminal for enabling the ~~first and second~~ switching ~~circuits~~ circuit to be ~~simultaneously~~ responsive to the voltage at the first terminal and (b) an output terminal, the output terminal of the ~~first~~ switching circuit being connected so current can flow via a ~~first~~ DC path between (a) the first power supply terminal and (b) the ~~first~~ capacitor and the gate electrode of the ~~first~~ transistor, ~~the output terminal of the second switching circuit being connected so current can flow via a second DC path between (a) the second power supply terminal and (b) the second capacitor and the gate electrode of the second transistor, the first and second~~ the DC ~~paths~~ path ~~respectively~~ including the first and second resistive ~~elements~~element.

Claim 8 [CURRENTLY AMENDED] The circuit of claim 7 wherein the ~~first and second~~ switching ~~circuits respectively include first and second inverters~~ circuit includes an inverter having field effect transistors.

Claim 9 [CURRENTLY AMENDED] The circuit of claim 8 wherein all ~~of~~ the field effect transistors are of the first inverter included on an integrated circuit chip including a ~~first and second resistors respectively~~ resistor comprising the ~~first and second~~ resistive element ~~elements~~ connected with the ~~first and second~~ field effect ~~transistors~~ transistor and the ~~first and second inverters~~inverter.

Claim 10 [CURRENTLY AMENDED] The circuit of claim 9 wherein the ~~first and second resistors are respectively~~resistor is included in the ~~first and second inverters~~inverter.

Claim 11 [CURRENTLY AMENDED] The circuit of claim 10 wherein ~~each of~~ the ~~inverters~~ inverter includes a PFET and an NFET, the PFET and NFET of ~~each~~ the inverter having a source drain path and a gate electrode having a connection to the first terminal so that the gate electrodes of the PFETs and NFETs of the ~~inverters~~ inverter are arranged to be driven in parallel

by the voltage at the first terminal, the output terminal of each of the inverters being between the source drain paths of the PFET and NFET thereof.

Claim 12 [CURRENTLY AMENDED] The circuit of claim 11 wherein the ~~first~~ resistor is connected between the source drain path of the NFET of the ~~first~~ inverter and the output terminal of the ~~first~~ inverter~~, the second resistor being connected between the source drain path of the PFET of the second inverter and the output terminal of the second inverter~~.

Claim 13 [CANCELED]

Claim 14 [CURRENTLY AMENDED] A circuit comprising a first terminal for connection to a voltage source having first and second levels and a transition between the levels, a driver including first and second opposite conductivity type transistors, each of the transistors including a control electrode and a path switched on and off in response to a voltage applied to the control electrode being on opposite sides of a threshold, the first and second transistor paths being connected in series across opposite power supply terminals, an output terminal between the paths, pulse shaping circuitry connected between the input terminal and the control electrodes for (a) causing the paths of the first and second transistors to be respectively (i) on and off while the voltage source has the first level and (ii) off and on while the voltage source has the second level, and (b) preventing the paths of the first and second transistors from being on simultaneously, the circuitry including: (a) first and second switching circuits arranged to be connected to be simultaneously responsive to the voltage at the first terminal, the first and second switching circuits respectively including output terminals that [[is]] are DC connected to the control electrodes of the first and second transistors; and (b) first and second capacitors that are respectively DC connected between (i) the first control electrode and the first power supply terminal and (ii) the second control electrode and the second power supply terminal, the first switching circuit including a first resistive element for supplying current from [[the]] a first power supply terminal of the power supply terminals to the control electrode of the first transistor and the first capacitor while the voltage at the first terminal has the first level, the first switching circuit being arranged for supplying a voltage substantially equal to the voltage at [[the]] a second power supply terminal of the power supply terminals to (i) the control electrode

of the first transistor and (ii) the first capacitor while the voltage at the first terminal has the second level; the second switching circuit including a second resistive element for supplying current from the second power supply terminal to the control electrode of the second transistor and the second capacitor while the voltage at the first terminal has the second level, the second switching circuit being arranged for supplying a voltage substantially equal to the voltage at the first power supply terminal to (i) the control electrode of the second transistor and (ii) the second capacitor while the voltage at the first terminal has the first level, the first switching circuit comprising: a first inverter including third and four transistors respectively switched on and off in response to the voltage at the first terminal respectively having first and second values, the first inverter including the first resistive element for supplying current from the first power supply terminal to the control electrode of the first transistor and the first capacitor while the third transistor is switched on; the second switching circuit comprises a second inverter including fifth and sixth transistors respectively switched on and off in response to the voltage at the first terminal respectively having first and second values, the second inverter including the second resistive element for supplying current from the second power supply terminal to the control electrode of the second transistor and the second capacitor while the sixth transistor is switched on, each of the inverters including a PFET and an NFET, the PFET and NFET of each inverter having a source drain path and a gate electrode having a connection to the first terminal so that the gate electrodes of the PFETs and NFETs of the inverters are arranged to be driven in parallel by the voltage at the first terminal, the output terminal of each of the inverters being between the source drain paths of the PFET and NFET thereof, the first ~~resistor~~resistive element being connected between the source drain path of the NFET of the first inverter and the output terminal ~~oft-he~~ of the first inverter, the second ~~resistor~~ resistive element being connected between the source drain path of the PFET of the second inverter and the output terminal of the second inverter.

Claim 15 [CANCELED]

Claim 16 (Previously Presented) The circuit of claim 14 wherein the fourth and fifth transistors while switched on are connected to supply voltages substantially at the second and

first power supply terminals to the control electrodes of the first and second transistors and the first and second capacitors, respectively.

Claim 17 (Original) The circuit of claim 16 wherein all the transistors and capacitors are field effect devices.

Claim 18 (previously presented) The circuit of claim 17 wherein all the transistors and capacitors are included on an integrated circuit chip, the first and second resistive elements including first and second resistors on the chip.

Claim 19 [CANCELED]

Claim 20 [NEW] A circuit comprising a first signal terminal for connection to a voltage source having first and second levels and a transition between the levels, a driver including a transistor having a first conductivity type, the transistor including a control electrode and a path arranged to be switched on and off in response to a voltage applied to the control electrode being on opposite sides of a threshold, the path being connected in series across first and second opposite power supply terminals, an output terminal coupled to the path, pulse shaping circuitry connected between the first signal terminal and the control electrode for (a) causing the path of the transistor to be on and off while the voltage source has the first and second levels; the circuitry including: (a) a switching circuit connected to be responsive to the voltage at the first terminal, the signal switching circuit including an output terminal that is DC connected to the control electrode of the first transistor; and (b) a capacitor that is DC connected between the control electrode and first of the power supply terminals, the switching circuit including a resistive element for supplying current from the first power supply terminal to the control electrode of the transistor and the capacitor while the voltage at the first signal terminal has the first level, the switching circuit being arranged for supplying a voltage substantially equal to the voltage at the second power supply terminal to (i) the control electrode of the first transistor and (ii) the first capacitor while the voltage at the first signal terminal has the second level; the first switching circuit comprising: a first inverter including second and third transistors respectively are arranged to be switched on and off in response to the voltage at the first signal terminal respectively having first and second values, the first inverter including the first resistive element

for supplying current from the first power supply terminal to the control electrode of the first transistor and the capacitor while the second transistor is switched on; the second and third transistors being respectively of the first conductivity type and a second conductivity type opposite to the first conductivity type, each of the second and third transistors having a source drain path and a gate electrode having a connection to the first terminal so that the gate electrodes of the second and third transistors are driven in parallel by the voltage at the first signal terminal, the output terminal of the inverter being between the source drain paths of the second and third transistors, the first resistive element being connected between the source drain path of the third transistor and the output terminal of the inverter.

Claim 21 [NEW] The circuit of claim 20 wherein the resistive element comprises a resistor.